Abstract—A high-speed low power scalable programmable dual modulus digital CMOS frequency divider architecture is proposed. The unique frequency divider architecture includes a high speed parallel counter with State Excitation Module, a switchover trigger circuit, a modulus switchover circuit and a reloader circuit. The mode switchover circuit has two sets of external programmable inputs for two alternative frequency select/modulus select. The reload circuit consists of a DFF, an inverter and a two input NAND gate. The reload circuit resets the parallel counter upon receiving the trigger pulses from the mode switch over circuit. Thus, the dual modulus digital CMOS frequency divider sequences through two alternative cycles and the number of states in each cycle is determined by the respective external inputs. Initially, the proposed dual modulus digital CMOS frequency divider was constructed using the existing parallel counter architecture [1]. Then, to improve the performance of the frequency divider circuit two different types of 8-bit counter architectures were proposed. The proposed dual modulus digital CMOS frequency divider using these two architectures provides improved performance compared to the same circuit by using the existing counter architecture. The 8-bit divider using the existing parallel counter architecture consumed a total transistor count of 780 whereas the same circuit using the proposed parallel counters consumed only 612 transistors. The power dissipation for divider using the existing parallel counter architecture and the proposed parallel counter architecture were 4.21mW ($P_{INT}$) and 3.60mW ($P_{INT}$) respectively at 250MHz. The worst case delay observed for divider using the existing parallel counter architecture and the proposed parallel counter architecture were 7.179ns and 7.164ns respectively using Altera Quartus II.

Keywords—Counter, divide-by-N, frequency divider, high speed, low-power, modules, modulus

I. INTRODUCTION

COUNTERS act as important building blocks for applications in fast arithmetic circuits such as frequency division, shifting operation etc. Frequency dividers are basic blocks in numerous numbers of applications, such as generation of clock pulses of desired frequency, synchronization and data recovery and frequency synthesis in satellite communication systems. An innovative design of a dual modulus digital CMOS frequency divider is carried out here. This unique frequency divider sequences through two alternative cycles and the number of states in each cycle is determined by the respective external inputs. It consists of a high speed parallel counter with State Excitation Module, a switchover trigger circuit, a mode switchover circuit and a reloader circuit. The counter blocks designed with low power consumption, high speed and less area requirement for a particular application. The counter blocks designed with low power consumption, high speed and less area requirement for a particular application. The counter blocks designed with low power consumption, high speed and less area requirement for a particular application. The counter blocks designed with low power consumption, high speed and less area requirement for a particular application. The counter blocks designed with low power consumption, high speed and less area requirement for a particular application.

S. Abdel-Hafeez et al. [2] proposed a simple implementation of frequency divider. However, the circuit had some design constraints to incorporate multiple frequency select inputs. In order to reduce high counter power consumption, Alioto et al. [3] presented a low power counter design with a relatively high operating frequency. Alioto’s design was based on cascading an analog block such that each counting stage’s input frequency was halved compared to the previous counting stage. However, Alioto’s counter design’s carry chain rippled through all counting stages, resulting in a total critical path delay equal to the sum of all counting stage delays. Subsequently, Alioto’s design was not well suited for large counter widths because the carry chain limited operating frequency even though the carry chain voltage was not rail-to-rail. A dual-modulus prescaler constructed with two parts-a synchronous counter and an asynchronous counter was proposed by B.Chang et al. [4]. But the advantage of reduction power consumption was negated by reduction in speed. Though it was a dual modulus divider, it won’t provide the option of selecting two modulus values externally. As a substitution to the carry chain, Kakarountas et al. [6] used a carry look-ahead circuit [5]. With the expense of an extra detector, the carry look-ahead circuit used a prescaler technique with systolic 4-bit counter modules using T-type flip-flops. The detector circuit output is used to enable counting in the higher order bits. Kakarountas’s design used DFFs between the counter modules to improve the operating speed of the parallel counter.

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frequency. As the counter design was limited by control signal broadcasting, Kakarountas’s design was not practical for large counter widths. Therefore a novel design of a dual modulus digital CMOS frequency divider which sequences through two alternative cycles whose modulus is determined by the two external inputs is proposed here. The remainder of the paper is organized as follows. Section II discusses about the proposed high speed parallel counter architectures. Section III provides an insight into the proposed dual modulus digital CMOS frequency divider architecture. Section IV provides a detailed discussion of the results and finally the conclusion is given in section V.

II. THE PROPOSED 8BIT PARALLEL COUNTER ARCHITECTURES

The major advantages of the proposed parallel counter architectures are listed below.

1) All the individual blocks in the counting path are designed by using JK flip-flops which reduces the number of gates required for its implementation. Therefore, the transistor count of the counting path is reduced.

2) In place for repeating counting blocks of equal width, the counting blocks of variable width is used to reduce the size of the state excitation module. This also reduces the transistor count and thereby the area required for the realization of the counter.

3) The proposed counter has an operating frequency that is almost independent of counter width as a single clock input triggers all counting modules simultaneously.

4) The counter output is in radix-2 representation so read on-the-fly of the count value is possible with no additional logic decoding.

5) For higher counter width the proposed parallel counter architecture offers the advantage of reusability of modules and thus reduces the design time.

Method I:

Fig. 1 shows the functional block diagram of the proposed high speed parallel counter using method I. It consists of two sections – The Counting Path and State Excitation Module.

I. Counting Path:

The counting path consists of four different modules. They are $M_{13}$, $DFF_{PS}$ and two subsequent counting modules ($M_{2KS}$). In the counting path the counting modules are separated by the pipelining flip-flops $DFF_{PS}$.

1) Module $M_{13}$: The module $M_{13}$ is a parallel synchronous 3-bit up counter using JK flip-flops. The schematic is shown in Fig.2. Here the J and K inputs of all the flip flops are shorted and $Q_{	ext{out}}(t+1) = JQ_{	ext{out}}(t) + K'Q_{	ext{out}}(t)$

$Q_{00}(t+1) = Q_{00}(t)$

$Q_{01}(t+1) = Q_{01}(t)$

$Q_{02}(t+1) = Q_{02}(t)$

$EN_{1} = Q_{01}Q_{00}$

The first three equations can be simplified as, $Q_{00}(t+1) = 1 \oplus Q_{00}(t)$

$Q_{01}(t+1) = Q_{00}(t) \oplus Q_{01}(t)$

$Q_{02}(t+1) = Q_{02}(t)$

The module $M_{13}$ is responsible for low-order bit counting and these three LSBs generate future states for all remaining modules in the counting path. In the counting path the enable output signal of module $M_{13}$ is pipelined through flip-flop $DFF_{P1}$ to enable the counting operation of the first subsequent counting module. Whenever the module $M_{13}$ output $Q_{00}Q_{01}Q_{02} = 110$, the input ST of the first subsequent counting module will be ‘1’ after a single clock pulse. The counting module will change its state only if ST=’1’. The connection between the basic and first subsequent counting module is such that when the basic module completes its full state sequence only, a single state change occurs for the first subsequent counting module.

i) Module $M_{2KS}$: The counting modules other than the basic module are represented here as $M_{2KS}$, where K represents the counter width of the counting module and S represents the position of the counting module after the basic module. The $M_{2KS}$ counting module will change its state only if ST=’1’. The two $M_{2KS}$ modules shown in fig.3 are modules $M_{221}$ and $M_{232}$ respectively. Here module $M_{221}$ is a two bit counting module and module $M_{232}$ is a three bit counting module.

Fig.3 depicts the schematic diagram of module $M_{221}$ and the output expressions are given by

$Q_{10}(t+1) = ST \oplus Q_{10}(t)$

$Q_{11}(t+1) = [ST Q_{10}(t)] \oplus Q_{11}(t)$

$EN_{21} = Q_{11}Q_{10}$

$Q_{10}(t+1) = ST \oplus Q_{10}(t)$

$Q_{11}(t+1) = [ST Q_{10}(t)] \oplus Q_{11}(t)$

$EN_{21} = Q_{11}Q_{10}$
Fig.4 depicts the schematic diagram of Module- \( M_{232} \) of the proposed high speed parallel counter (Method I) and the output expressions are given by

\[
Q_{20}(t+1) = ST \ XOR \ Q_{20}(t)
\]

\[
Q_{21}(t+1) = [ST Q_{20}(t)] \ XOR \ Q_{21}(t)
\]

\[
Q_{22}(t+1) = [ST Q_{21}(t) Q_{20}(t)] \ XOR \ Q_{22}(t)
\]

\[
EN_{22} = Q_{22} Q_{21} Q_{20}
\]

State Excitation Module (SEM):

The State Excitation Module consists of a D flipflop \( DFF_{SEM} \) a three input AND gate and an inverter. It decodes the count states of module \( M_{13} \). This decoding is carried over two clock cycles through two DFFs (\( DFF_{SEM} \) of SEM and the second pipelining flip-flop \( DFF_{P2} \) of the counting path) to trigger the second subsequent module \( M_{232} \). In fig. 1, the counting path’s first D flip-flop (\( DFF_{P1} \)) decodes the low-order state \( Q_{02} Q_{01} Q_{00} = 110 \) and carries this decoding across one clock cycle and enables \( Q_{11} Q_{10} = 01 \) at module \( M_{221} \) on the next rising clock edge. The State Excitation Module decodes the low-order state \( Q_{02} Q_{01} Q_{00} = 101 \) and carries this decoding over two cycles. By Combining the one cycle mechanism in the counting path for \( Q_{11} Q_{10} = 10 \) and a two-cycle mechanism for \( Q_{02} Q_{01} Q_{00} = 101 \), \( Q_{22} Q_{21} Q_{20} \) can be enabled. Thus all modules to be triggered concurrently on the clock edge, thus avoiding any rippling or long frequency delay. Fig. 5 shows the measured waveforms of the High Speed Counter using Altera Quartus II simulator at 250MHz.
Figure 5. Measured waveforms of the proposed High Speed Counter using Altera Quartus II simulator at 250MHz

Method II:

Fig. 6 shows the functional block diagram of the proposed high speed parallel counter using method II. Similar to the parallel counter in fig. 1, it consists of two sections – The Counting Path and State Excitation Module.

1. Counting Path:

The counting path consists of three different modules. They are $M_{13}$, $DFF_{Ps}$, and two subsequent counting modules ($M_{2KS}$). Similar to method I, here also the counting modules are separated by the pipelining flip-flops $DFF_{Ps}$ in the counting path.

i) Module- $M_{13}$

The module $M_{13}$ is a parallel synchronous 2-bit up counter using JK flip-flops. The schematic is shown in Fig.7. Here the J and K inputs of the flip flops are shorted and thus its operation is equivalent to a T flip-flop. The logic expressions of the outputs of the basic module $M_{13}$ are given by,

$Q_{00}(t+1) = J_0Q'_{00}(t) + K'_{0}Q_{00}(t)$ (15)

$Q_{01}(t+1) = Q_{00}(t)Q'_{01}(t) + Q'_{00}(t)Q_{01}(t)$ (16)

$EN_1= Q_{01} Q'_{00}$ (17)

The equations (9) and (10) can be simplified as,

$Q_{00}(t+1) = 1 \ xor Q_{00}(t)$ (18)

$Q_{01}(t+1) = Q_{00}(t) \ xor Q_{01}(t)$ (19)

The module $M_{13}$ is responsible for low-order bit counting and these two LSBs generate future states for all remaining modules in the counting path. In the counting path the enable output signal of module $M_{13}$ is pipelined through flipflop $DFF_{P1}$ to enable the counting operation of the first subsequent counting module. Whenever the module $M_{13}$ output $Q_{00}Q_{00} =10$, the input ST of the first subsequent counting module will be ‘1’ after a single clock pulse. The counting module will change its state only if ST='1'. The connection between the basic and first subsequent counting module is such that when the basic module completes its full state sequence only, a single state change occurs for the first subsequent counting module.

i) Module- $M_{2KS}$

Fig.8 depicts the schematic diagram of module $M_{2KS}$. The two $M_{2KS}$ modules shown in fig.8 are modules $M_{231}$ and $M_{232}$ respectively.

The output expressions of module $M_{231}$ are given by,

$Q_{10}(t+1)= ST \ xor Q_{10}(t)$ (20)

$Q_{11}(t+1)= [STQ_{10}(t)] \ xor Q_{11}(t)$ (21)

$Q_{12}(t+1)= [STQ_{11}(t) Q_{10}(t)] \ xor Q_{12}(t)$ (22)

$EN_{21}= Q_{12}Q_{11} Q_{10}$ (23)

Similarly, the output expressions of module $M_{232}$ are given by,

$Q_{20}(t+1)= ST \ xor Q_{20}(t)$ (24)

$Q_{21}(t+1)= [STQ_{20}(t)] \ xor Q_{21}(t)$ (25)

$Q_{22}(t+1)= [STQ_{21}(t) Q_{20}(t)] \ xor Q_{22}(t)$ (26)

$EN_{22}= Q_{22}Q_{21} Q_{20}$ (27)

State Excitation Module (SEM):

The State Excitation Module consists of a D flip-flop $DFF_{SEM}$, a two input AND gate and an inverter. It decodes the count states of module $M_{13}$. The State Excitation Module of the proposed high speed parallel counter of fig.6 decodes the count states of its basic module, $M_{13}$. This decoding is carried over two clock cycles through two $DFF_{Ps}$ of $DFF_{SEM}$ and the second pipelining flip-flop $DFF_{P2}$ of the counting path to trigger the second subsequent module $M_{232}$. In fig. 6, the counting path’s first D flip-flop ($DFF_{P1}$) decodes the low-order state $Q_{00}Q_{00} =10$ and carries this decoding across one clock cycle and enables $Q_{12}Q_{11}Q_{10} =001$ at module $M_{231}$ on the next rising clock edge. The State Excitation Module decodes the low-order state $Q_{00}Q_{00} =00$ and carries this decoding over two cycles. By Combining the one cycle mechanism in the counting path for $Q_{12}Q_{11}Q_{10} =110$ and a two-cycle mechanism for $Q_{00}Q_{00} =01$, $Q_{22}Q_{21}Q_{20}$ can be enabled. Thus all modules are triggered concurrently on the clock edge, avoiding any rippling or long frequency delay.
Fig. 9 shows the measured waveforms of the High Speed Counter using Altera Quartus II simulator at 250MHz.

III. THE PROPOSED DUAL MODULUS DIGITAL CMOS FREQUENCY DIVIDER

Most divide-by-N programmable frequency dividers [2] consist of a counter, a reload circuit, and an end of count detector with external programmable inputs for frequency select. Fig.10 shows the Functional block diagram of the proposed Dual Modulus Digital CMOS Frequency Divider. This special frequency divider architecture proposed here is structured with a counter, a switch over trigger circuit, a mode switchover circuit with two sets of external programmable inputs for two alternative frequency select/modulus select and a reload circuit. The counter used is a high speed parallel counter with State Excitation Module. This high speed counter is very effective for performing the divide-by-N frequency function as all binary counts happen simultaneously at the edge of the input clock frequency. The mode switchover circuit (Fig.11) in conjunction with the switchover trigger circuit and the reload circuit allows the counter to proceed with its state sequence from zero to N1 (represents the first external input P7P6P5P4P3P2P1P0) at first and then with the state sequence from zero to N2 (represents the second external input S7S6S5S4S3S2S1S0). The reload circuit consists of a DFF and gates G1 and G2.

Operation of the dual modulus digital CMOS frequency divider

Fig.12 shows the measured waveforms of the dual modulus digital CMOS frequency divider using Altera Quartus II simulator. The waveform shows that the counter sequences through two alternative cycles (N1='00000111' and N2='00001111'). If the reset input RES=1 and clock signal is given the counter starts from state '00000000' to '00000111'. Once it reaches the state ‘00000111’ the reloader circuit gets activated and the counter enters into reset state. From there it proceeds up to the state ‘00001111’ which constitutes the second cycle. Once it reaches the state ‘00001111’ the reloader circuit gets activated and the counter again enters into reset state. From there it counts up to the
state ‘0000111’. In short the counter sequences through two alternative cycles and the number of states in each cycle is determined by the two external inputs. i.e, N1 = ‘P7P6P5P4P3P2P1P0’ and N2 = ‘S7S6S5S4S3S2S1S0’.

The output equation of the mode switch over circuit for S=0 is given by,

\[
Q = (P0 \oplus Q0)(P1 \oplus Q1)(P2 \oplus Q2)(P3 \oplus Q3)
\]
\[
(P4 \oplus Q4)(P5 \oplus Q5)(P6 \oplus Q6)(P7 \oplus Q7) 
\]  
(28)

The output equation of the mode switch over circuit for S=1 is given by,

\[
Q = (S0 \oplus Q0)(S1 \oplus Q1)(S2 \oplus Q2)(S3 \oplus Q3)
\]
\[
(S4 \oplus Q4)(S5 \oplus Q5)(S6 \oplus Q6)(S7 \oplus Q7) 
\]  
(29)

The 8-bit mode switchover circuit consists of an inverter, 16 numbers of 2-input AND gates, 8 numbers of 2-input OR gates, 8 numbers of 2-input XNOR gates and an 8-input AND gate. Therefore a generalized n-bit mode switchover circuit consists of an inverter, ‘2n’ numbers of 2-input AND gates, ‘n’ numbers of 2-input OR gates, ‘n’ numbers of 2-input XNOR gates and an n-input AND gate. Fig.13 shows the functional block diagram of the generalized n-bit Dual Modulus Digital CMOS Frequency Divider circuit.
both the J and K inputs connected together. The clear input of the flip-flop is also connected with the J and K inputs so that it toggles only when IN='1'. The ‘Q’ output of the D flip-flop in fig. 13 is given to the input ‘CLKIN’ of the switch over circuit.

![Figure 13. The functional block diagram of the generalized n-bit Dual Modulus Digital CMOS Frequency Divider circuit.](image)

![Figure 14. The schematic diagram of the n-bit mode switchover circuit](image)

![Figure 15. The schematic diagram of the switchover trigger circuit](image)

**IV. RESULTS AND DISCUSSIONS**

In this section the performance of the Dual Modulus Digital CMOS Frequency Divider circuit is analyzed. Note that for all the observations the device cyclone EP1C20F400C7 is used here. Table I shows the Transistor Count of the proposed Dual Modulus Digital CMOS Frequency Divider (Using parallel counter of existing method). The total transistor count is 780 in which the transistor count of the counter, mode switch over circuit, switch over trigger circuit and reload circuit are 442, 292, 20 and 26 respectively. The Power dissipation of the counter at 250 MHz was found to be 3.54 mW (P_{INT}). The measured values of the high speed parallel counter (existing) using Altera Quartus II simulator are listed in Table II. The worst case delay measured of the proposed Dual Modulus Digital CMOS Frequency Divider using Altera Quartus II simulator was found to 7.179 ns. The Power dissipation at 250 MHz was found to be 4.21 mW (P_{INT}). The measured values the proposed Dual Modulus Digital CMOS Frequency Divider (Using parallel counter of existing method) using Altera Quartus II simulator are listed in Table III.

**TABLE I. TRANSISTOR COUNT OF THE PROPOSED DUAL MODULUS DIGITAL CMOS FREQUENCY DIVIDER (USING PARALLEL COUNTER OF EXISTING METHOD[1])**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor count</th>
<th>Power Dissipation (P_{INT})</th>
</tr>
</thead>
<tbody>
<tr>
<td>442</td>
<td>3.54 mW</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE II. PERFORMANCE ANALYSIS OF THE HIGH SPEED PARALLEL COUNTER (USING EXISTING METHOD[1])**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor count</th>
<th>Power Dissipation (P_{INT})</th>
<th>Delay (worst case)</th>
</tr>
</thead>
<tbody>
<tr>
<td>780</td>
<td>4.21 mW</td>
<td>7.179 ns</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE III. PERFORMANCE ANALYSIS OF THE DUAL MODULUS DIGITAL CMOS FREQUENCY DIVIDER (USING PARALLEL COUNTER OF EXISTING METHOD[1])**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor count</th>
<th>Power Dissipation (P_{INT})</th>
<th>Delay (worst case)</th>
</tr>
</thead>
<tbody>
<tr>
<td>780</td>
<td>4.21 mW</td>
<td>7.179 ns</td>
<td></td>
</tr>
</tbody>
</table>

Table IV shows the Transistor Count of the proposed Dual Modulus Digital CMOS Frequency Divider (Using parallel counter of method I). The total transistor count is 612 in which the transistor count of the counter, mode switch over circuit, switch over trigger circuit and reload circuit are 274, 292, 20 and 26 respectively. The Power dissipation of the counter at 250 MHz was found to be 2.19 mW (P_{INT}). The measured values of the high speed parallel counter (method I) using Altera Quartus II simulator are listed in Table V. The worst case delay measured of the proposed Dual Modulus Digital CMOS Frequency Divider using Altera Quartus II simulator was found to 7.164 ns. The Power dissipation at 250 MHz was found to be 3.60 mW (P_{INT}).

<table>
<thead>
<tr>
<th>Modules</th>
<th>8-bit counter</th>
<th>Mode switch over circuit</th>
<th>Switch over trigger circuit</th>
<th>Reload circuit</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor count</td>
<td>442</td>
<td>292</td>
<td>20</td>
<td>26</td>
<td>780</td>
</tr>
</tbody>
</table>


Table VII, VIII and IX shows the Transistor Count of the proposed Dual Modulus Digital CMOS Frequency Divider (Using parallel counter of method II), the measured values of the high speed parallel counter (method II), and the measured values of the proposed Dual Modulus Digital CMOS Frequency Divider (Using parallel counter of method II) respectively.

Finally, all the important results of the proposed Dual Modulus Digital CMOS Frequency Divider using the three different counter architectures are summarized in Table X.

### Table VI. Performance Analysis of the Proposed High Speed Parallel Counter (Method I)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor count</th>
<th>Delay (worst case)</th>
<th>Power Dissipation (P_INT)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>274</td>
<td>6.737 ns</td>
<td>2.91 mW</td>
</tr>
</tbody>
</table>

### Table VII. Performance Analysis of the Proposed High Speed Parallel Counter (Method II)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor count</th>
<th>Power Dissipation (P_INT)</th>
<th>Delay (worst case)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>612</td>
<td>3.60 mW</td>
<td>7.164 ns</td>
</tr>
</tbody>
</table>

### Table VIII. Performance Analysis of the Proposed Dual Modulus Digital CMOS Frequency Divider (Using Parallel Counter of Method II)

<table>
<thead>
<tr>
<th>Modules</th>
<th>8-bit counter</th>
<th>Mode switch over circuit</th>
<th>Switch over trigger circuit</th>
<th>Reload circuit</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
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<td>274</td>
<td>292</td>
<td>20</td>
<td>26</td>
<td>612</td>
</tr>
</tbody>
</table>

### Table IX. Performance Analysis of the Proposed Dual Modulus Digital CMOS Frequency Divider (Using Parallel Counter of Method II)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor count</th>
<th>Power Dissipation (P_INT)</th>
<th>Delay (worst case)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>612</td>
<td>3.60 mW</td>
<td>7.164 ns</td>
</tr>
</tbody>
</table>

### Table X. Performance Analysis of the Dual Modulus Digital CMOS Frequency Divider Circuits

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transistor count</th>
<th>Delay (worst case)</th>
<th>Power Dissipation (P_INT)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>274</td>
<td>6.737 ns</td>
<td>2.91 mW</td>
</tr>
</tbody>
</table>
V. CONCLUSION

In this paper, a high speed low power Dual Modulus Digital CMOS Frequency Dividers is presented along with various parallel counter architectures. The divider structure is implemented for a size of 8-bit, which provides varied frequency dividing factors from 2 to 255. The Dual Modulus Digital CMOS Frequency Divider with parallel counter using existing method[1] has a total transistor count of 780 where as those with the proposed counter architectures have only 612. Altera Quartus II simulation results show that the Dual Modulus Digital CMOS Frequency Divider with parallel counter using existing method[1] has a power dissipation of 4.21mW(PINT) at 250MHz where as those with the proposed counter architectures have only 3.60mW(PINT) at the same frequency. The worst case delay of 7.179ns was observed for the Dual Modulus Digital CMOS Frequency Divider with parallel counter using existing method[1] and 7.164ns each for the Dual Modulus Digital CMOS Frequency Divider with parallel counter using the two proposed methods. In short, a reduction in area (transistor count) by 21.53%, reduction in power dissipation by 14.49% and reduction in delay by 0.21% is achieved for the proposed Dual Modulus Digital CMOS Frequency Divider by replacing the existing counter by the proposed counter architectures. Also the proposed Dual Modulus Digital CMOS Frequency Divider circuits show improved performance in terms of power consumed, delay and area compared to its previous counterpart.

REFERENCES

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